Gold damascene interconnect technology for millimeter-wave photonics on silicon

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ABSTRACT

Thick-gold-multilevel damascene-interconnect technology makes it possible to fabricate >10-μm-feature ultrahigh-speed devices on Si. Adding H_2O_2 to a conventional KIO_3-based slurry triples the removal rate of gold in chemical mechanical polishing (CMP). A ratio of H_2O_2 to slurry of ~1:1 is found to be the optimum for obtaining the highest gold removal rate. X-ray photoelectron spectroscopy (XPS) analyses show that gold is oxidized in spite of its chemical stability when the removal rate is high. The gold is oxidized due to the reduction of iodine at the optimum H_2O_2 mixture ratio. This CMP of gold enabled us to make a thick (>10 μm) gold-multilevel damascene-interconnection structure for the first time. Integration of full-wafer wafer-bonded uni-traveling carrier photodiodes (UTC-PDs) with the gold multilevel interconnections as coplanar waveguides (CPWs) on a Si wafer has been achieved using this gold-CMP process.

Keywords: millimeter-wave, Si, CMP, gold, damascene, interconnection, UTC-PD, CPW, wafer bonding

1. INTRODUCTION

During the past several decades, Si technology has made great progress, leading to the development of ultralarge-scale integrated circuits (ULSIs) in microelectronics. Because of Si technology's maturity and low cost for practical use, there is strong desire to implement new functions on a chip by combining Si devices with sensors, microelectromechanical systems (MEMS), radio-frequency (RF) devices, and millimeter-wave (MMW) photonic devices.[1-6] However, from the viewpoint of device features, there is a technology gap in the 10-μm region (Fig. 1) because recent ULSI processes aimed at submicrometer-feature devices are not suitable for fabricating new larger devices. New and practical ways of fabrication based on Si technology applicable in the several-ten μm region are therefore urgently necessary so that we may seamlessly combine new electrical and heterogeneously functional devices with smaller and larger electrical devices. We call such technologies **sea**mless **i**ntegration **t**echnology, or "*SeaiT*".[3,7]

The wave of technological fusion is indeed sweeping over RF applications and MMW photonics.[8-10] The development of RF and millimeter-wave integrated systems is now within the range of Si-core technologies[7,11] as the result of the introduction of high-speed Si-based devices like sub-0.1-μm LSIs[12] and SiGe ICs,[13,14] and the ability to combine compound semiconductors and Si by full-wafer wafer bonding.[15] Then, the key components in these high- and ultrahigh-speed systems -components such as antennas, filters, and transmission lines- need to be made on silicon connecting to such high speed active devices. In making these components, we need to reduce the conductor loss from interconnections and reduce the dielectric loss caused by interlayer films and substrates.

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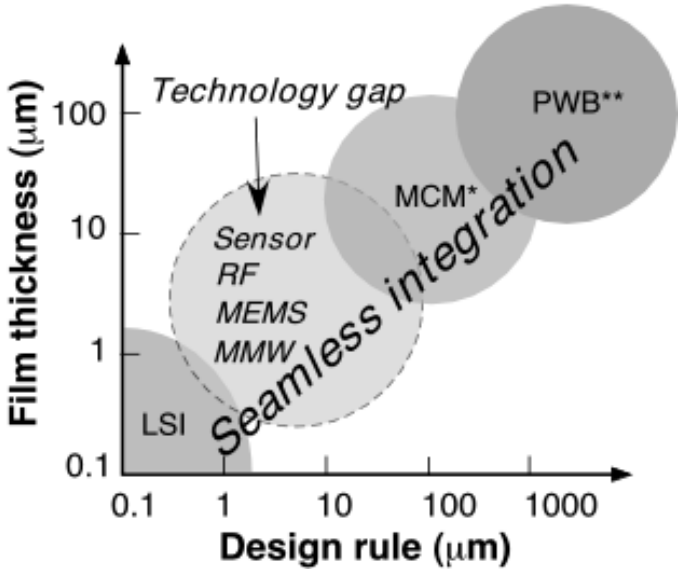

Fig. 1: Device-feature-based technology classification.
*multi-chip module, **printed wired board

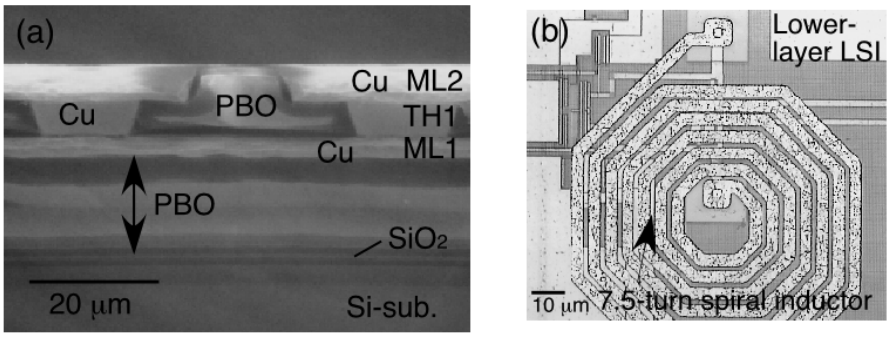

Fig. 2: Cu RF devices using SeaiT: (a) Cross-sectional SEM image of thick-Cu interconnections, (b) top view of Cu-spiral inductor made on a LSI.

For the combination of RF devices with ULSIs, we developed a multilevel thick-Cu damascene interconnect technology that uses electroless-plated Ru/Ni caps on Cu interconnections as oxidation protection layers and photosensitive polybenzoxazole (PBO) as interlayer dielectrics (Fig. 2).[2,3,16] In this damascene structure, low-resistive thick-Cu interconnection is separated from Si by thick interlayer dielectric to reduce the influence of Si. Such a structure has low conductor loss and low dielectric loss. Cu has very low resistivity indeed; however, in much higher frequency regions, such as the millimeter-wave region where the skin effect has a large influence on signal transmission, Cu interconnections are inappropriate as transmission lines because of their chemical instability. For instance, oxidation converts Cu surface region from a conductor to an insulator.

As mentioned above, multilevel interconnection using low-resistivity material and the damascene structure is an effective way to reduce conductor loss and dielectric loss in high-speed systems on Si. For low conductor loss, gold is one of the most promising materials because of its low resistivity and chemical stability. However, gold's chemical stability itself has prevented the damascene structure formation because it has not been possible to obtain a high-removal rate in chemical mechanical polishing (CMP), which is necessary if damascene process is to be of practical use.

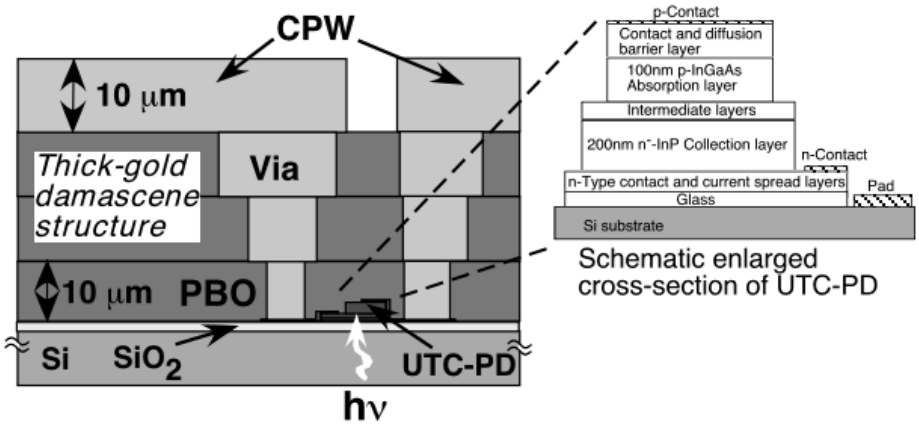

Fig. 3: Schematic cross-section of MMW-CPW integrated with UTC-PD on Si.

We have succeeded in tripling its removal rate by simply adding hydrogen peroxide to conventional alumina slurry. This enables us to form a thick gold damascene structure. This paper describes a combination of electronics and photonics: multilevel thick-gold damascene interconnect technology for MMW transmission lines as coplanar waveguides (CPWs) and their integration with wafer-bonded uni-traveling carrier photodiode (UTC-PD)[17] on Si (Fig. 3). Device fabrication processes are described first. Then, the gold CMP process is examined on the basis of x-ray photoelectron spectroscopy (XPS). Finally, gold damascene transmission lines as CPWs integrated with UTC-PDs on a Si are evaluated by electro-optic sampling technique.

2. FABRICATION

2.1 Process flow

Figure 4 shows the device fabrication process. The whole process was performed on full 2-inch wafers. The first stage is the wafer-bonded UTC-PD fabrication on high resistivity silicon wafer (~3 kΩcm). The epitaxial layers of UTC-PD were grown on InP substrate by metal-organic chemical vapor deposition (MOCVD). Wafer bonding was then performed by using a sodium silicate glass intermediate layer.[3,6] After InP substrate removal, the conventional UTC-PD process was carried out and the Au/Pt/Ti electrode was formed [Fig. 4(a)]. A schematic of the wafer-bonded device structure is shown in Fig. 3.

The second stage is the fabrication of the vias to connect the wafer-bonded UTC-PD and upper CPWs. This was accomplished with three levels of damascene PBO-imbedded thick (10 μm) gold to form the connection to the UTC-PD [Fig. 4(b)-(f)]. The final stage is thick gold electroplating to form the CPW [Fig. 4(g)].

The details of the thick-gold damascene structure processes are as follows. Vias to the below interconnections were formed by photolithographic patterning of a spincoated positive-photosensitive PBO layer [Fig. 4(b)]. The positive photosensitive nature of PBO allows us to make vias, interconnection patterns, and interlayer dielectrics simultaneously. The Au(70 nm)/Ti(100 nm) was successively deposited by evaporation. Ti and Au work as an adhesive for the PBO and a seed layer for electroplating, respectively.

Then the resist was spincoated and patterned to restrict the gold electroplating area [Fig. 4(c)]. This area-restriction makes the CMP easier because it reduces planarization area and increases pressure. In our via pattern, this area restriction increased the gold-removal rate by about 30 times compared to the gold-removal rate of whole surface. The gold electroplating was carried out using $Na_3Au(SO_3)_2$, which is less toxic than gold cyanide. The via holes were filled with gold and the 10-μm-high gold protrusion was formed [Figs. 4(d) and (e)].

The gold protrusion was planarized by CMP with a 1:1 mixture of conventional KIO_3-based slurry (RODEL SWA2000) and commercially available 35%-H_2O_2aq after removal of the area-restricted resist [Figs. 4(e) and (f)]. Adding H_2O_2 to the conventional slurry tripled the gold-removal rate. Figure 5 compares the gold-removal rate with and without H_2O_2 addition. Without H_2O_2, it took one hour to polish the gold knob even using area-restriction. On the other hand, with H_2O_2, it took only 20 min. We repeated this gold-via forming process three times to make 3-level multilevel interconnections. Each layer was 10-μm thick. Despite the total thickness of the PBO and the novelty of the gold CMP process, the PBO film was damage-free. Combining the area-restriction and H_2O_2 addition in gold CMP accelerates the removal rate by up to 90 times. We were thus able to make the first-ever thick-gold multilevel-damascene structure.

The 10-μm-thick layers of gold were electroplated in the patterned resist. Finally, the resist was removed and the CPWs were formed on 30-μm-thick PBO [Fig. 4 (g)]. This completes the fabrication process. Figure 6 shows (a) a top view and (b) a cross-sectional image of the fabricated device. The flat interface shown in Fig 6(b) demonstrates the effectiveness of this H_2O_2-added CMP of gold. And the CPWs are formed 30 μm from the Si substrate.

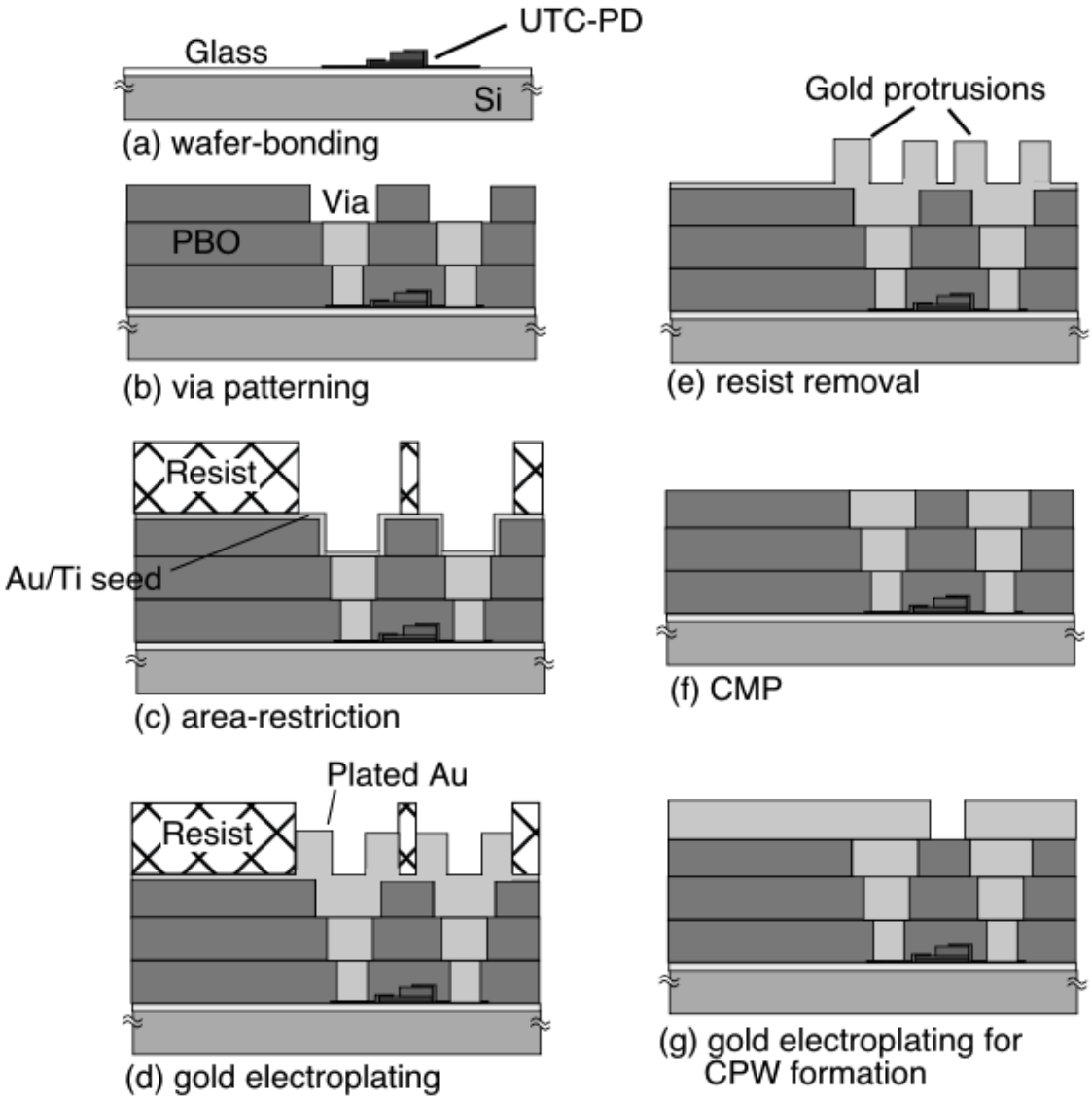

Fig. 4: Processes for thick-gold damascene structure fabrication.

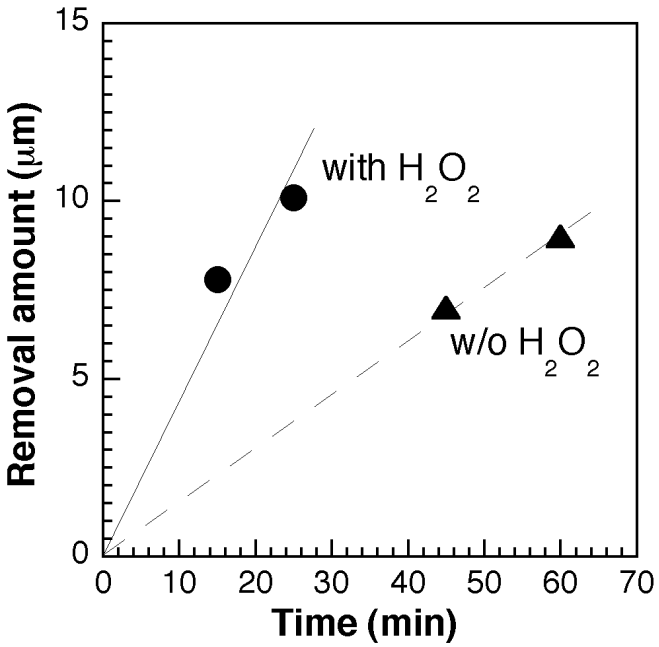

Fig. 5: Comparison of removed amount of gold with and without H_2O_2.

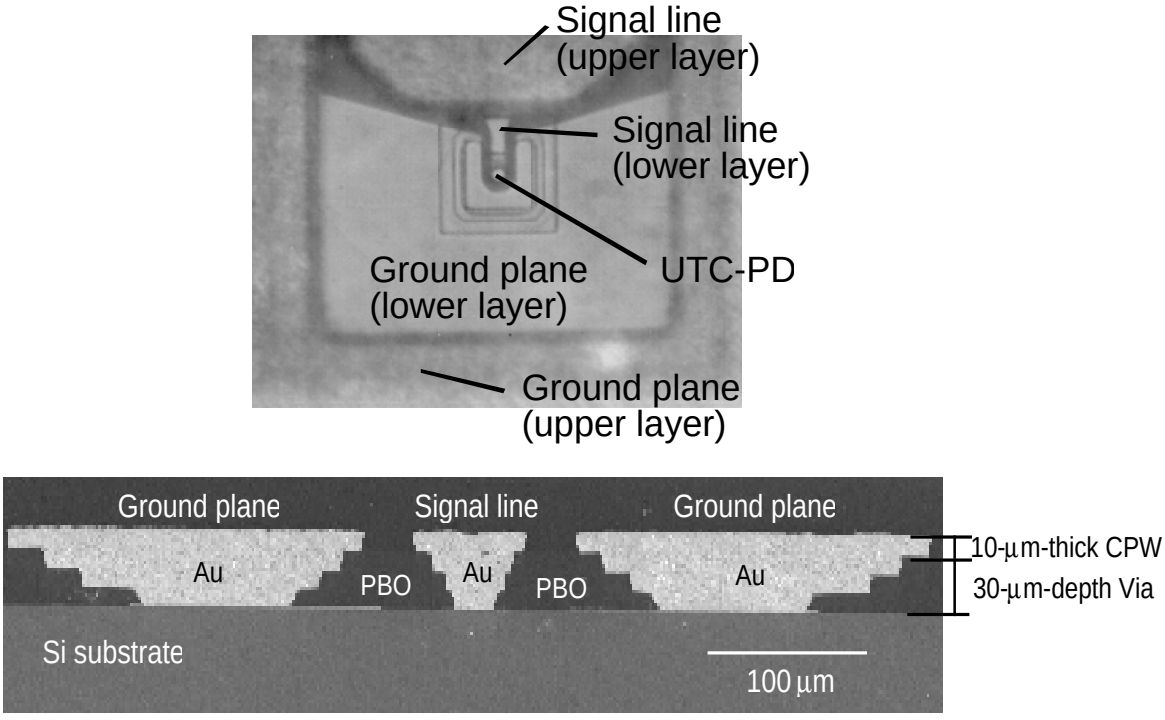

Fig. 6: Images of fabricated device: (a) Top view of the device, (b) cross-sectional SEM image of gold CPW fabricated far from Si substrate.

2.2 Characteristics of gold CMP

This section describes how the removal rate of chemically stable gold is accelerated in CMP just by adding H_2O_2 to a KIO_3-based slurry (RODEL MSW2000). In this section, we used 6-inch Si wafers and CMP was carried out on the whole gold surface of the wafer. Consequently, the polishing rate is smaller than that mentioned in the former section where CMP was performed on the (area-restricted) gold protrusions.

Figure 7 shows the time dependence of the amount of gold removed. The amount has a linear relationship with polishing time for 40 min. The fact that there is no saturation of the removed amount during such a long polishing means that the chemical conditions on the gold surface during CMP remain constant. We investigated the H_2O_2-mixture ratio dependence on the removal rate. Figure 8 indicates that the relationship between the gold-removal rate and concentration of 35%-H_2O_2aq to the total-slurry volume. The removal rate steeply rises to a maximum value of 35 nm/min at a ~50%-mixture concentration and falls to ~10 nm/min at a 62.5%-mixture concentration. This means that chemical conditions vary according to H_2O_2 addition.

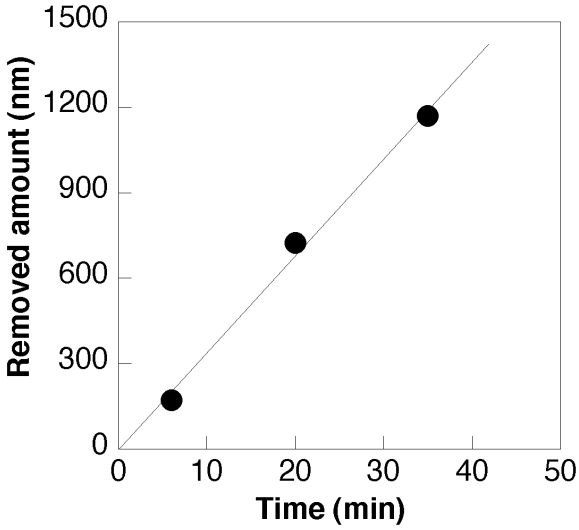

Fig. 7: Time dependence of removal rate. MSW2000 : H_2O_2 = 1:1

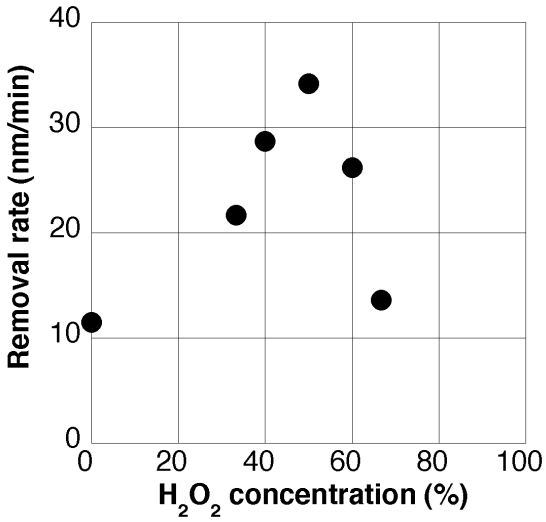

Fig. 8: Relationship between gold removal rate and H_2O_2 mixture concentration.

To clarify the mechanisms of the H_2O_2-added gold CMP, we measured XPS spectra of the abrasive during CMP. During the CMP, we gathered some abrasive with a pipette and passed it by a suction filter. After drying in the air, the abrasive was transferred into the XPS apparatus. X-ray source was AlKα line (1486.6 eV). Figure 9 shows the XPS spectra for the Au4f region. The spectra for Figs. 9(a), (b), (c) correspond to the abrasive gathered at H_2O_2-mixture concentration of 60, 50, 0%, respectively. Figure 9(d) is for reference as-plated gold. It is observed that Au4f photoelectron intensity correlates qualitatively to the gold removal rate. The full width at half maximum (FWHM) of the Au4f7/2 for spectrum (b) is 1.5 eV and that for as-plated gold is 1.0 eV. This means that during CMP, gold is removed in the form of some compounds. The spectrum for (b) shifts to the 0.5-eV-higher binding energy side compared to the spectrum for (d) of as-plated gold. This further shows that the compounds are in an oxidized state. That is, H_2O_2-addition causes some oxidized gold compounds to form when the gold removal rate is high in spite of gold's chemical stability.

Figure 10 shows the XPS spectra for the I3d region. Iodine is derived from the conventional slurry containing KIO_3. Spectra (a), (b), and (c) also correspond to the abrasive gathered at H_2O_2-mixture concentration of 60, 50, 0%, respectively. For spectra (a) and (c) at low removal rate, we can observe both oxidized iodine with the valence state of 5+ and non-oxidized iodine. On the other hand, for spectra (b) at high removal rate, almost no oxidized iodine is observed. That is, iodine of IO_3^- ion is reduced to I^0 and gold is oxidized to $Au^{\delta+}$ with the 50%-H_2O_2 addition as shown in Fig. 9(b). Gold oxidation and iodine reduction have a flip-flop relationship.

It is known that chemical oscillation of IO_3^-/I_2 catalyzed H_2O_2 decomposition occurs[18] according to reactions (1) and (2) shown in Fig. 11. H_2O_2 produces nascent oxygen that has strong oxidation ability and iodine to react with IO_3^- in reaction (1). H_2O_2 and the produced iodine produce IO_3^- in turn according to reaction (2). Because of the small free-energy difference between reactions (1) and (2), the two reactions cause chemical oscillation. In our system, according to reaction (3) in Fig. 11, the oxidation of gold might occur due to the nascent oxygen produced by reaction (1). The flip-flop relationship of the observed redox reaction in gold and iodine is thought to be derived from this IO_3^-/I_2 catalyzed H_2O_2 decomposition. Although further study is necessary in order to clarify the mechanisms by which H_2O_2 is incorporated into this redox system, it is apparent at present that the acceleration of the removal rate is achieved by the chemical equilibrium of H_2O_2 and KIO_3 and gold. Actually, we confirmed that no acceleration of the gold removal rate occurs without KIO_3 even when H_2O_2 is added to the slurry.

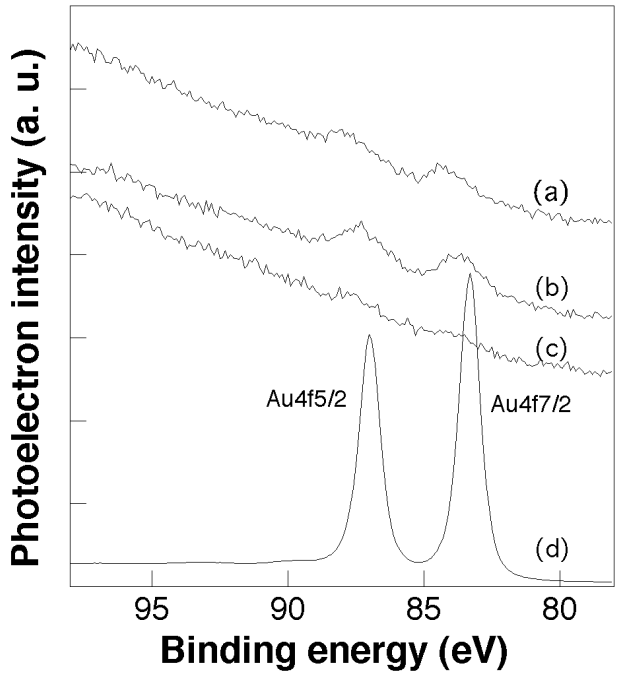

Fig. 9: Au4f XPS spectra of abrasive during CMP. H_2O_2 concentration is 60, 50, 0% for spectra (a), (b), and (c), respectively. Spectrum (d) is for as-plated gold.

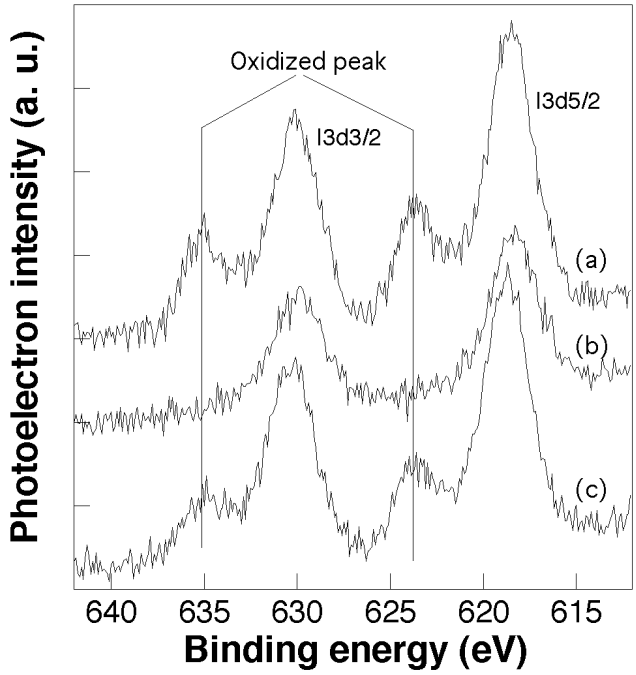

Fig. 10: I3d XPS spectra of abrasive during CMP. H_2O_2 concentration is 60, 50, 0% for spectra (a), (b), and (c), respectively.

$$5H_2O_2 + 2HIO_3 \longrightarrow 10O^* + I_2 + 6H_2O \quad (1)$$

Chemical oscillation

$$I_2 + 5H_2O_2 \longrightarrow 2HIO_3 + 4H_2O \quad (2)$$

$$Au + xO^* \longrightarrow AuOx \quad (3)$$

Fig. 11: Reactions for gold oxidation: (1) and (2) are oscillation reactions for IO_3^-/I_2 catalyzed decomposition of H_2O_2. (3) Oxidation of gold by nascent oxygen. Asterisk * stands for nascent state.

3. EVALUATION

The gold CPWs integrated on Si with wafer-bonded UTC-PDs were characterized by the electro-optic sampling (EOS) technique.[19] Figure 12 is a schematic diagram of the measurement system. In this measurement, 1.55-μm-wavelength 500-fs light pulses were input into a UTC-PD from the rear side of the Si wafer. The generated electrical pulse from the UTC-PD, which corresponds to >100-GHz MMW, propagating along the CPW was measured at different distances from the device with a CdTe electro-optic sensor. The CPWs on PBO, which are separated by 30 μm from Si by this multilevel-damascene structure were compared with CPWs formed directly on high-resistivity silicon (without the multilevel-damascene structure) on the same wafer. Figure 13 compares the MMW propagation along the CPW from the device with and without the multilevel damascene structure. Waveforms were measured at 0 and 2 mm from the device. Signal propagating on the CPW fabricated directly on silicon (without the PBO multilevel-damascene structure) has a peak output reduction of 29.8% and 16.6-ps duration. For the CPW fabricated on 30-μm-thick PBO (with the multilevel-damascene structure), the amplitude is decreased by 13.6% and the duration is 11.7 ps. Amplitude reduction and duration are smaller for the CPW made with the multilevel-damascene structure. These results indicate that the effect of Si substrate is decreased by separating the CPWs from the Si substrate by gold multilevel-damascene structure and this structure is an effective approach to achieve excellent transmission characteristics for the MMW region.

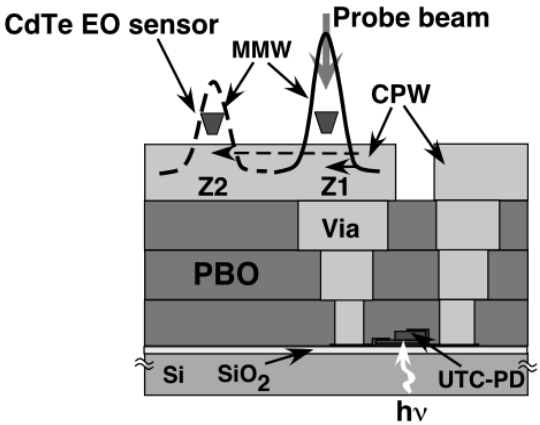

Fig. 12: Schematic diagram for EO measurement setup.

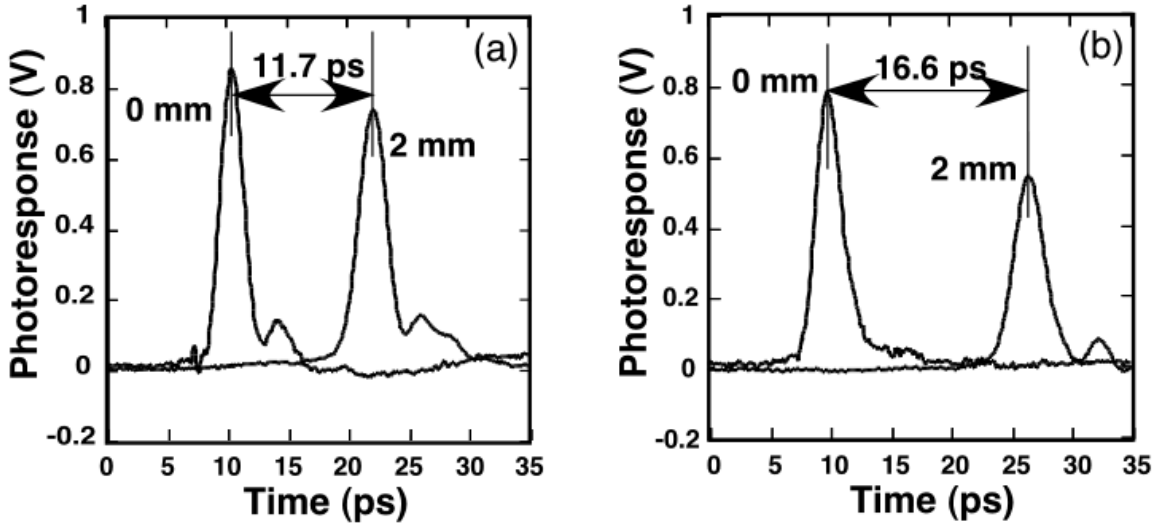

Fig. 13: MMW transmission characteristics for CPW made on Si (a) with and (b) without the gold multilevel damascene structure. Characteristic impedance was 50Ω for each CPW. MMW was measured by EOS at Z1 = 0 mm and Z2 = 2 mm. Z1 and Z2 are defined in Fig. 12.

4. SUMMARY

We have tripled the removal rate of gold in CMP by adding H_2O_2 to the conventional KIO_3 based slurry. We found there is optimum ratio of slurry to H_2O_2 for obtaining high-removal rate of gold. An XPS analysis demonstrated that the gold is oxidized in a mixture of H_2O_2 and slurry when the removal rate is high. This might be the reason for the accelerated gold removal rate. The redox relationship between gold and iodine is in the flip-flop mode and seems to be based on the chemical equilibrium between H_2O_2, KIO_3 and gold. The first-ever practical fabrication method for >10 μm-thick gold-damascene structure is thus achieved by this high-removal-rate gold CMP. Applying this CMP and thick-PBO processes, we have fabricated thick-gold multilevel-damascene interconnections as CPWs integrated with UTC-PDs on a Si. We confirmed their effectiveness for MMW transmission by electro-optic sampling. Seamless integration technology paves the way for the fusion of silicon devices with other new functions.

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